WHAT IS CLAIMED IS:

1. A method for controlling the slew rate of a signal driven by a signal driver characterized by an output impedance onto a transmission line of an integrated circuit device, comprising:

determining a desired slew rate for said signal;

calculating characteristic capacitance which together with said signal driver output impedance will produce a resulting time constant on said transmission line to achieve said desired slew rate;

calculating an interconnection path characterized by a redistribution metal characteristic capacitance substantially equal to said calculated characteristic capacitance;

connecting said signal driver to a first end of said interconnection path; and

connecting said transmission line to said second of said interconnection path.

2. A method in accordance with claim 1, wherein:

said characteristic capacitance is selected such that for a desired 95% full signal transition time *t*, *t* is approximately equal to $3*R_O*C_{RM}$, where R_O comprises said signal driver output resistance and C_{RM} comprises said characteristic capacitance.

3. An integrated circuit device, comprising:

a signal driver which drives a signal onto a transmission line;

redistribution metal connecting said signal driver to said transmission line, said redistribution metal characterized by a capacitance which causes a desired slew rate on said transmission line when said signal transitions from a first state to a second state.

4. An integrated circuit device in accordance with claim 3, wherein:

said characteristic capacitance comprises a value C_{RM} such that for a desired 95% full signal transition time *t*, *t* is approximately equal to $3*R_O*C_{RM}$, where R_O comprises said signal driver output resistance.

5. A method for mapping a signal driver of an integrated circuit to one of a plurality of interconnect pads, comprising:

determining an output impedance of said signal driver;

determining a desired slew rate for a signal generated by said signal driver;

calculating a desired characteristic capacitance, said desired characteristic capacitance having a capacitance value which together with said output impedance of said signal driver will provide a resulting characteristic time constant required to achieve said desired slew rate on a transmission line connected to receive said signal;

calculating at least one possible interconnection path to each said plurality of interconnect pads;

estimating a characteristic capacitance associated with each said at least one possible interconnection paths;

selecting one of said possible interconnection path whose associated characteristic capacitance is substantially equal to said desired characteristic capacitance; and

mapping said output driver to said interconnection pad associated with said selected interconnection path.

6. A method in accordance with claim 5, comprising:

connecting said signal driver to a first end of said selected interconnection path; and

connecting said interconnection pad to a second of said selected interconnection path.

7. A method in accordance with claim 5, wherein:

said desired characteristic capacitance is selected such that for a desired 95% full signal transition time *t*, *t* is approximately equal to

$3*R_O*C_{RM}$, where R_O comprises said signal driver output resistance and C_{RM} comprises said characteristic capacitance.